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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,236	08/28/2003	Tatsutoshi Abe	393032040300	6413

7590 02/03/2011

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ART UNIT	PAPER NUMBER
2451	

MAIL DATE	DELIVERY MODE
02/03/2011	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/650,236
Filing Date: August 28, 2003
Appellant(s): ABE ET AL.

Peng Li
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/12/2010 appealing from the Office action mailed 3/15/2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-2 and 4-10.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6148051	Fujimori et al.	11/2000
2002/0064185 A1	Nakai et al.	5/2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 4-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fujimori et al.** (hereinafter **Fujimori**) U.S. Patent No.: 6,148,051 and further in view of **Nakai et al.** (hereinafter **Nakai**) U.S. Publication No.: 2002/0064185 A1.

Regarding **Claim 1(and 2, 8 & 10) Fujimori** discloses: A command synchronization establishment system comprising:

a network wherein a cycle master node managing time on the network periodically transmits a cycle start packet including time information to each node

connected to the network, each node synchronizes its clock in accordance with the time information included in the cycle start packet so as to assure isochronism on the network by sharing the synchronized clock with each other node **(Fujimori: Figures 1- 6 and Col. 6 lines 13- 21; master node, cycle time extracting circuit, cycle start packet and cycle packet train)**.

However, **Fujimori** does not appear to explicitly disclose the specific teachings of data is transferred by an isochronous transfer, and a command is transferred by an asynchronous transfer using a time period after the isochronous transfer until the next cycle start packet;

a controller as a node connected to the network, comprising a transmitter that transmits a command including a time-stamp based on the synchronized clock to a target apparatus by using the asynchronous transfer; and

the target apparatus as another node connected to the network, comprising a receiver that receives the command, a storage device that temporally stores the received command in order not to execute the received command instantly, a transmitter that transmits an interim response to the controller reflecting that the received command will be executed when a current time based on the synchronized clock reaches a time represented by the time-stamp included in the command, an executing device that executes the received command when the current time based on the synchronized clock reaches the time represented by the time-stamp included in the command, and a replying

device that provides a complete response indicating completion of executing the command.

In the same field of endeavor, **Nakai** discloses an data is transferred by an isochronous transfer, and a command is transferred by an asynchronous transfer using a time period after the isochronous transfer until the next cycle start packet **(Nakai: Figures 18 and par. 13, 24 and 152; command content and asynchronous band)**;

a controller as a node connected to the network, comprising a transmitter that transmits a command including a time-stamp based on the synchronized clock to a target apparatus by using the asynchronous transfer **(Figures 2, 5 and 18 and par. 13, 24 and 152; command content, time stamps and asynchronous transmission)**; and

the target apparatus as another node connected to the network, comprising a receiver that receives the command, a storage device that temporally stores the received command in order not to execute the received command instantly, a transmitter that transmits an interim response to the controller reflecting that the received command will be executed when a current time based on the synchronized clock reaches a time represented by the time-stamp included in the command, an executing device that executes the received command when the current time based on the synchronized clock reaches the time represented by the time-stamp included in the command **(Figures 6-14, 18 & 24 and par. 152, 163 & 168; request/response nodes, executing content**

when reaching the received time and time stamps), and a replying device that provides a complete response indicating completion of executing the command **(Figures 18 & 24 and par. 152- 153; request/response nodes and acknowledgement packets)**.

Accordingly it would have been obvious for one of ordinary skill in the networking art to modify or incorporate **Nakai's** teachings of waiting until the time stamp time before executing an action with the teachings of **Fujimori**, to provide for a more efficiency in synchronizing systems.

Regarding **claim 4 Fujimori-Nakai** further discloses:

wherein said each node connected to the network shares the synchronized clock with each other node by copying the time information included in the cycle start packet to a cycle time register in each node, and said time-stamp included in the command is in a format including a part or all formats of the cycle time register **(Figures 1-5B and Abstract & Col. 4 lines 8-26; time stamp register, cycle timing register, cycle period, clock generating circuit and delay and comparing circuit and synchronizing internal time data)**.

Regarding **claim 5 Fujimori-Nakai** further discloses:

wherein said command includes a flag instructing the executing device to execute the command instantly or when the current time reaches the time represented by the time-stamp included in the command, and the target apparatus determines whether to execute the received command instantly or when the current time reaches the time represented by the time-stamp in

accordance with the flag **(Nakai: Figures 18- 25 and Par. 152; time stamps, acknowledgement packets and waiting until time stamp time and starting action)**.

Regarding **claim 6 Fujimori-Nakai** further discloses:

wherein the flag uses a part of a format of the time-stamp included in the command **(Figures 1-5B and Abstract & Col. 4 lines 8-26; time stamp register, receipt register, time register, cycle timing, cycle period, clock generating circuit and delay and comparing circuit and data packets and synchronizing internal time data)**.

Claim 7 is substantially the same as **claims 1- 2, 4- 6, 8 and 10**, but in method form rather than system form, and is therefore rejected using the same rationale as in **claims 1- 2, 4- 6, 8 and 10**.

Claim 9 is substantially the same as **claims 1- 2, 4- 6, 8 and 10**, but in apparatus form rather than system form, and is therefore rejected using the same rationale as in **claims 1- 2, 4- 6, 8 and 10**.

Examiner Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in its entirety as potentially teaching of all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner.

(10) Response to Argument

In substance appellant argues that Fujimori and Nakai, whether alone or in combination, fail to disclose or suggest: A) a transmitter that transmits an interim

response to the controller reflecting that the received command will be executed when a current time based on the synchronized clock reaches a time represented by the time-stamp included in the command; B) a replying device that provides a complete response indicating completion of executing the command.

In response to A), the examiner respectfully disagrees. Appellant's recitation of an “interim response” is broad. As such the examiner understands this interim response to be any form or communication/transaction (i.e., an acknowledgment, calculation and/or step) that reflects (i.e., some how shows, exhibits and/or expresses) that a received command will be executed when a current time based on the synchronized clock reaches a time represented by the time-stamp included in the command. The examiner would like to bring to attention at least the following two points:

- Nakai’s disclosure of the various ways and steps to determining delay between two nodes (Nakai at least in figures 6-14), and then transmitting the value for the calculated delay to the requesting node in order to express (i.e. reflect) that a command be executed at the indicated time within a time-stamp.
- Appellant’s point, on page 5 of the instant Brief--referencing paragraphs 152-153 of Nakai-- “that the response node N2 receives a command with a time stamp therein from the request node N1 and executes the command at the time indicated by the time stamp.”

Hence, Nakai discloses a form of communication/transaction (i.e., an acknowledgment, calculation and/or step)--as in calculating delay--that reflects

(i.e., some how shows, exhibits and/or expresses) that a received command will be executed when a current time based on the synchronized clock reaches a time represented by the time-stamp included in the command—as in using/utilizing this time delay/deviation to determine the exact time to execute a command.

In response to B), the examiner respectfully disagrees. Once again, appellant's use of the term indicating is broad, and as such is understood by the examiner to mean (and/or be synonymous with) hinting, signing, signaling and or suggesting. As such the examiner contends, and as appellant points out on page 5 of the instant Brief--referencing Nakai figures 24-- the use of acknowledgment packets. These, packets are used to indicate the completion of a transaction, as in acknowledging the receipt of a packet/communication. As such the examiner contends, keeping in mind the points made in response to A) above (i.e., that a command is executed at the time indicated by the time stamp etc.), and that in isochronous communication it is guaranteed that data transmission is completed in every 125 micro-seconds (Nakai par. 14); that an acknowledgment packet received towards the end of this cycle (125 micro-seconds) would indicate/hint to the completion of a command.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

M.A.

/John Follansbee/

Supervisory Patent Examiner, Art Unit 2451

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